WHAT IS CLAIMED IS:

1. In a circuit comprising at least one MOS transistor and external circuitry to forward bias a well of said MOS transistor, a method of biasing said well comprising:

determining a bias current to be drawn from said well; and

biasing said well by drawing said determined bias current from said well with said external circuitry.

2. The method of Claim 1, wherein said external circuitry comprises a transistor.

3. The method of Claim 1, wherein said circuit comprises a differential amplifier.

4. A differential amplifier circuit, comprising:

a first MOS transistor formed in a well and comprising a gate terminal configured as a first input to the differential amplifier, and a source terminal;

a second MOS transistor formed in a well and comprising a gate terminal configured as a second input to the differential amplifier, and a source terminal coupled to said source terminal of said first MOS transistor, wherein said well of said first MOS transistor is coupled to said well of said second MOS transistor;

a third MOS transistor comprising a source terminal coupled to a voltage source and a drain coupled to said source terminals of said first and second MOS transistors; and

a transistor current source coupled to at least said well of said first MOS transistor so as to draw a current from said well.

5. The amplifier of Claim 4, wherein said transistor current source is coupled to said well of said second MOS transistor so as to draw a current from said well.

6. A circuit comprising two or more transistors formed in wells coupled to different biasing circuits, wherein a current drawn from the wells is substantially the same, and wherein the well potentials are different.

7. The circuit of Claim 6, wherein at least one of said biasing circuits comprises a transistor coupled to at least one of the wells and configured to draw a current from the well.

8. A method of reducing the operating voltage level of an integrated circuit comprising at least one group of two or more transistors, wherein said transistors are formed in wells, said method comprising forward biasing said transistor wells with a common current but not a common potential.

9. A plurality of integrated circuits fabricated from a series of different wafers subject to process variations during wafer production, at least a portion of said integrated circuits from said series of different wafers sharing a common layout of a plurality of MOS transistors comprising wells;

wherein said wells on each wafer are connected to current sources on each wafer, and

wherein said current sources are configured to forward bias said wells by drawing substantially the same current from said wells, irrespective of any resulting inter-wafer or intra-wafer differences in the source to well voltage produced by said current due to process variations affecting the physical structure of the MOS transistors within or between wafers.